Syllabus of
UNDERGRADUATE DEGREE COURSE

Electronics Instrumentation & Control

Rajasthan Technical University, Kota
Effective from session: 2021 – 2022
# 3EI2-01: Advance Engineering Mathematics-I

**3 Credits**

<table>
<thead>
<tr>
<th>SN</th>
<th>Contents</th>
<th>Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td><strong>Laplace Transform:</strong>&lt;br&gt;Definition and existence of Laplace transform, Properties of Laplace Transform and formulae, Unit Step function, Dirac Delta function, Heaviside function, Laplace transform of periodic functions. Finding inverse Laplace transform by different methods, convolution theorem. Evaluation of integrals by Laplace transform, solving ODEs by Laplace transforms method.</td>
<td>10</td>
</tr>
<tr>
<td>4</td>
<td><strong>Fourier Transform:</strong>&lt;br&gt;Fourier Complex, Sine and Cosine transform, properties and formulae, inverse Fourier transforms, Convolution theorem, application of Fourier transforms to partial ordinary differential equation (One dimensional heat and wave equations only).</td>
<td>7</td>
</tr>
<tr>
<td>5</td>
<td><strong>Z-Transform:</strong>&lt;br&gt;Definition, properties and formulae, Convolution theorem, inverse Z-transform, application of Z-transform to difference equation.</td>
<td>5</td>
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<td><strong>Total</strong></td>
<td><strong>40</strong></td>
</tr>
</tbody>
</table>
### 3EI1-02/4EI1-02: Technical Communication

**2 Credit**

**Max. Marks: 100 (IA:30, ETE:70)**

**End Term Exam: 2 Hours**

<table>
<thead>
<tr>
<th>SN</th>
<th>Contents</th>
<th>Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><strong>Introduction to Technical Communication</strong>- Definition of technical communication, Aspects of technical communication, forms of technical communication, importance of technical communication, technical communication skills (Listening, speaking, writing, reading writing), linguistic ability, style in technical communication.</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td><strong>Comprehension of Technical Materials/Texts and Information Design &amp; development</strong>- Reading of technical texts, Reading and comprehending instructions and technical manuals, Interpreting and summarizing technical texts, Note-taking. Introduction of different kinds of technical documents, Information collection, factors affecting information and document design, Strategies for organization, Information design and writing for print and online media.</td>
<td>6</td>
</tr>
<tr>
<td>3</td>
<td><strong>Technical Writing, Grammar and Editing</strong>- Technical writing process, forms of technical discourse, Writing, drafts and revising, Basics of grammar, common error in writing and speaking, Study of advanced grammar, Editing strategies to achieve appropriate technical style, Introduction to advanced technical communication. Planning, drafting and writing Official Notes, Letters, E-mail, Resume, Job Application, Minutes of Meetings.</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td><strong>Advanced Technical Writing</strong>- Technical Reports, types of technical reports, Characteristics and formats and structure of technical reports. Technical Project Proposals, types of technical proposals, Characteristics and formats and structure of technical proposals. Technical Articles, types of technical articles, Writing strategies, structure and formats of technical articles.</td>
<td>8</td>
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<td></td>
<td><strong>Total</strong></td>
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</tbody>
</table>
## Contents

<table>
<thead>
<tr>
<th>SN</th>
<th><strong>Basic economic concepts</strong>- Meaning, nature and scope of economics, deductive vs inductive methods, static and dynamics, Economic problems: scarcity and choice, circular flow of economic activity, national income-concepts and measurement.</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td><strong>Demand and Supply analysis</strong>- Demand-types of demand, determinants of demand, demand function, elasticity of demand, demand forecasting –purpose, determinants and methods, Supply-determinants of supply, supply function, elasticity of supply.</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td><strong>Production and Cost analysis</strong>- Theory of production- production function, law of variable proportions, laws of returns to scale, production optimization, least cost combination of inputs, isoquants. Cost concepts-explicit and implicit cost, fixed and variable cost, opportunity cost, sunk costs, cost function, cost curves, cost and output decisions, cost estimation.</td>
<td>5</td>
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<tr>
<td>4</td>
<td><strong>Market structure and pricing theory</strong>- Perfect competition, Monopoly, Monopolistic competition, Oligopoly.</td>
<td>4</td>
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<tr>
<td>5</td>
<td><strong>Financial statement analysis</strong>- Balance sheet and related concepts, profit and loss statement and related concepts, financial ratio analysis, cash-flow analysis, funds-flow analysis, comparative financial statement, analysis and interpretation of financial statements, capital budgeting techniques.</td>
<td>8</td>
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</tbody>
</table>

**Total** 26
3EI4-04: Digital System Design

3 Credits

Max. Marks: 100 (IA:30, ETE:70)

End Term Exam: 3 Hours

<table>
<thead>
<tr>
<th>SN</th>
<th>Contents</th>
<th>Hours</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>Logic Simplification and Combinational Logic Design: Review of Boolean Algebra and De Morgan’s Theorem, SOP &amp; POS forms, Canonical forms, Karnaugh maps up to 6 variables, Binary codes, Code Conversion.</td>
<td>7</td>
</tr>
<tr>
<td>2</td>
<td>MSI devices like Comparators, Multiplexers, Encoder, Decoder, Driver &amp; Multiplexed Display, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Barrel shifter and ALU</td>
<td>8</td>
</tr>
<tr>
<td>3</td>
<td>Sequential Logic Design: Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF, Ripple and Synchronous counters, Shift registers, Finite state machines, Design of Synchronous FSM, Algorithmic State Machines charts. Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation.</td>
<td>9</td>
</tr>
<tr>
<td>4</td>
<td>Logic Families and Semiconductor Memories: TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out, Tristate TTL, ECL, CMOS families and their interfacing, memory elements, Concept of Programmable logic devices like FPGA. Logic implementation using programmable devices.</td>
<td>8</td>
</tr>
<tr>
<td>5</td>
<td>VLSI Design flow: Design entry: Schematic, FSM &amp; HDL, different modeling styles in VHDL, Data types and objects, Dataflow, Behavioral and Structural Modeling, Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.</td>
<td>8</td>
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</tbody>
</table>

Total 40
## Course Outcome:

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Name</th>
<th>Course Outcome</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>3EI4-04</td>
<td>Digital System Design</td>
<td>CO 1</td>
<td>Develop the understanding of number system and its application in digital electronics.</td>
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<tr>
<td></td>
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<td>CO 2</td>
<td>Development and analysis of K-map to solve the Boolean function to the simplest form for the implementation of compact digital circuits.</td>
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<td>CO 3</td>
<td>Design various combinational and sequential circuits using various metrics: switching speed, throughput/latency, gate count and area, energy dissipation and power.</td>
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<td>CO 4</td>
<td>Understanding Interfacing between digital circuits and analog component using Analog to Digital Converter (ADC), Digital to Analog Converter (DAC) etc.</td>
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<td>CO 5</td>
<td>Design and implement semiconductor memories, programmable logic devices (PLDs) and field programmable gate arrays (FPGA) in digital electronics.</td>
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</tbody>
</table>

## CO-PO Mapping:

<table>
<thead>
<tr>
<th>Subject</th>
<th>Course Outcomes</th>
<th>PO 1</th>
<th>PO 2</th>
<th>PO 3</th>
<th>PO 4</th>
<th>PO 5</th>
<th>PO 6</th>
<th>PO 7</th>
<th>PO 8</th>
<th>PO 9</th>
<th>PO 10</th>
<th>PO 11</th>
<th>PO 12</th>
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<td>3EI4-04</td>
<td>CO 1</td>
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</table>

3: Strongly 2: Moderate 1: Weak
### Lecture Plan:

<table>
<thead>
<tr>
<th>Lecture No.</th>
<th>Content to be taught</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lecture 1</td>
<td>Zero Lecture</td>
</tr>
<tr>
<td>Lecture 2</td>
<td>Review of Boolean Algebra</td>
</tr>
<tr>
<td>Lecture 3</td>
<td>DeMorgan’s Theorem, SOP &amp; POS forms,</td>
</tr>
<tr>
<td>Lecture 4</td>
<td>Problem of SOP and POS forms of boolean functions.</td>
</tr>
<tr>
<td>Lecture 5</td>
<td>Simplification of karnaugh map up to 6 variables</td>
</tr>
<tr>
<td>Lecture 6</td>
<td>Simplification of karnaugh map up to 6 variables</td>
</tr>
<tr>
<td>Lecture 7</td>
<td>Simplification of karnaugh map up to 6 variables</td>
</tr>
<tr>
<td>Lecture 8</td>
<td>Binary codes and code conversion</td>
</tr>
<tr>
<td>Lecture 9</td>
<td>Binary codes and code conversion</td>
</tr>
<tr>
<td>Lecture 10</td>
<td>Encoder, Decoder</td>
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<tr>
<td>Lecture 11</td>
<td>Half and Full Adders, Subtractors, Serial and Parallel Adders</td>
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<tr>
<td>Lecture 12</td>
<td>BCD Adder, Barrel shifter</td>
</tr>
<tr>
<td>Lecture 13</td>
<td>S-R FF, edge triggered and level triggered</td>
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<tr>
<td>Lecture 14</td>
<td>D and J-K FF</td>
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<tr>
<td>Lecture 15</td>
<td>Master-Slave JK FF and T FF</td>
</tr>
<tr>
<td>Lecture 16</td>
<td>Ripple and Synchronous counters</td>
</tr>
<tr>
<td>Lecture 17</td>
<td>Other type of counters</td>
</tr>
<tr>
<td>Lecture 18</td>
<td>Shift registers, Finite state machines, Asynchronous FSM</td>
</tr>
<tr>
<td>Lecture 19</td>
<td>Design of synchronous FSM</td>
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<tr>
<td>Lecture 20</td>
<td>Design of synchronous FSM</td>
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<tr>
<td>Lecture 21</td>
<td>Design of synchronous FSM</td>
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<tr>
<td>Lecture 22</td>
<td>Designing synchronous circuits (pulse train generator, pseudo random binary sequence generator, clock generation)</td>
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<tr>
<td>Lecture</td>
<td>Topic</td>
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<tr>
<td>23</td>
<td>TTL NAND gate, specifications, noise margin, propagation delay, fan-in, fan-out</td>
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<tr>
<td>24</td>
<td>TTL NAND gate</td>
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<tr>
<td>25</td>
<td>Tristate TTL, ECL</td>
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<tr>
<td>26</td>
<td>CMOS families and their interfacing</td>
</tr>
<tr>
<td>27</td>
<td>CMOS families and their interfacing</td>
</tr>
<tr>
<td>28</td>
<td>Read-Only Memory, Random Access Memory</td>
</tr>
<tr>
<td>29</td>
<td>Programmable Logic Arrays (PLA)</td>
</tr>
<tr>
<td>30</td>
<td>Programmable Array Logic (PAL),</td>
</tr>
<tr>
<td>31</td>
<td>Field Programmable Gate Array (FPGA)</td>
</tr>
<tr>
<td>32</td>
<td>Combinational PLD-Based State Machines,</td>
</tr>
<tr>
<td>33</td>
<td>State Machines on a Chip</td>
</tr>
<tr>
<td>34</td>
<td>Schematic, FSM &amp; HDL</td>
</tr>
<tr>
<td>35</td>
<td>Different modeling styles in VHDL</td>
</tr>
<tr>
<td>36</td>
<td>Data types and objects, Data flow</td>
</tr>
<tr>
<td>37</td>
<td>Behavioral and Structural Modeling</td>
</tr>
<tr>
<td>38</td>
<td>Behavioral and Structural Modeling</td>
</tr>
<tr>
<td>39</td>
<td>Simulation VHDL constructs and codes for combinational and sequential circuits</td>
</tr>
<tr>
<td>40</td>
<td>Simulation VHDL constructs and codes for combinational and sequential circuits</td>
</tr>
</tbody>
</table>

**Content delivery method:**

1. Chalk and Duster
2. PPT
3. Hand-outs
### Sample Assignments:

**Assignment 1**

**Q1.** Using K-maps, find the minimal Boolean expression of the following SOP and POS representations.
   a. \( f(w,x,y,z) = \Sigma (7,13,14,15) \)
   b. \( f(w,x,y,z) = \Sigma (1,3,4,6,9,11,14,15) \)
   c. \( f(w,x,y,z) = \Pi(1,4,5,6,11,12,13,14,15) \)
   d. \( f(w,x,y,z) = \Sigma (1,3,4,5,7,8,9,11,15) \)
   e. \( f(w,x,y,z) = \Pi (0,4,5,7,8,9,13,15) \)

**Q2.** Find the function \( h(a,b,c,d) \) such that \( f = f^a \).
   \( f(a,b,c,d) = a \cdot b \cdot c + (a \cdot c + b) \cdot d + h(a,b,c,d) \)

**Q3.** Using K-maps of the functions \( f_1 \) and \( f_2 \), find the following:
   (provide the canonical form expression and simplify)
   a. \( T_1 = f_1 \cdot f_2 \)
   b. \( T_2 = f_1 + f_2 \)
   c. \( T_3 = f_1 \oplus f_2 \)
   where \( f_1(w,x,y,z) = \Sigma (0,2,4,9,12,15) \), \( f_2(w,x,y,z) = \Sigma (1,2,4,5,12,13) \)

**Assignment 2**

**Q1.** Draw the state diagram of a serial adder.

**Q2.** In the following circuit, given binary values were applied to the Inputs \( X \) and \( Y \) inputs of the NAND latch shown in the figure. \( X = 0, Y = 1; X = 0, Y = 0; X = 1, Y = 1 \). Find out the corresponding stable output \( P, Q \).
<table>
<thead>
<tr>
<th><strong>Q3.</strong></th>
<th>When the race around condition will occur in the circuit given below:</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Circuit Diagram" /></td>
<td></td>
</tr>
</tbody>
</table>
RAJASTHAN TECHNICAL UNIVERSITY, KOTA
SYLLABUS
2nd Year - III Semester: B.Tech. (Electronics Instrumentation & Control)

3EI4-05: Signals & Systems
3 Credits
Max. Marks: 100 (IA:30, ETE:70)
3L:0T:0P
End Term Exam: 3 Hours

<table>
<thead>
<tr>
<th>SN</th>
<th>Contents</th>
<th>Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Energy and power signals, continuous and discrete time signals, continuous and discrete amplitude signals. System properties: linearity: additivity and homogeneity, shift-invariance, causality, stability, realizability.</td>
<td>6</td>
</tr>
<tr>
<td>3</td>
<td>Periodic and semi-periodic inputs to an LSI system, the notion of a frequency response and its relation to the impulse response, Fourier series representation, the Fourier Transform, convolution/multiplication and their effect in the frequency domain, magnitude and phase response, Fourier domain duality. The Discrete-Time Fourier Transform (DTFT) and the Discrete Fourier Transform (DFT). Parseval's Theorem. The idea of signal space and orthogonal bases</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>The Laplace Transform, notion of eigen functions of LSI systems, a basis of eigen functions, region of convergence, poles and zeros of system, Laplace domain analysis, solution to differential equations and system behavior.</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>The z-Transform for discrete time signals and systems - eigen functions, region of convergence, z-domain analysis.</td>
<td>5</td>
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<td></td>
<td>Total</td>
<td>40</td>
</tr>
</tbody>
</table>
### Course Outcome:

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Name</th>
<th>Course Outcome</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>3E1405</td>
<td>Signals &amp; Systems</td>
<td>CO 1</td>
<td>Analyze different types of signals and system properties</td>
</tr>
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<td></td>
<td></td>
<td>CO 2</td>
<td>Represent continuous and discrete systems in time and</td>
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<td>frequency domain using different transforms</td>
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<td>CO 3</td>
<td>Investigate whether the system is stable.</td>
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<td>CO 4</td>
<td>Sampling and reconstruction of a signal.</td>
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<td>CO 5</td>
<td>Acquire an understanding of MIMO systems</td>
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</tbody>
</table>

### CO-PO Mapping:

<table>
<thead>
<tr>
<th>Subject</th>
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<th>PO 1</th>
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<td>3E1405 Signals &amp; Systems</td>
<td>CO 1</td>
<td>3</td>
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</tbody>
</table>

**3: Strongly**  **2: Moderate**  **1: Weak**
### Lecture Plan:

<table>
<thead>
<tr>
<th>Lecture No.</th>
<th>Content to be taught</th>
</tr>
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<tbody>
<tr>
<td>Lecture 1</td>
<td>Zero Lecture</td>
</tr>
<tr>
<td>Lecture 2</td>
<td>Energy signals power signals</td>
</tr>
<tr>
<td>Lecture 3</td>
<td>Continuous and discrete time signals</td>
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<tr>
<td>Lecture 4</td>
<td>Continuous amplitude signals</td>
</tr>
<tr>
<td>Lecture 5</td>
<td>and discrete amplitude signals</td>
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<tr>
<td>Lecture 6</td>
<td>System properties: linearity: additivity and homogeneity</td>
</tr>
<tr>
<td>Lecture 7</td>
<td>shift-invariance, causality</td>
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<tr>
<td>Lecture 8</td>
<td>stability, realizability.</td>
</tr>
<tr>
<td>Lecture 9</td>
<td>Linear shift-invariant (LSI) systems</td>
</tr>
<tr>
<td>Lecture 10</td>
<td>impulse response</td>
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<tr>
<td>Lecture 11</td>
<td>Step response</td>
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<tr>
<td>Lecture 12</td>
<td>Convolution.</td>
</tr>
<tr>
<td>Lecture 13</td>
<td>Input output behavior with aperiodic convergent inputs</td>
</tr>
<tr>
<td>Lecture 14</td>
<td>Characterization of causality and stability of linear shift-invariant systems.</td>
</tr>
<tr>
<td>Lecture 15</td>
<td>System representation through differential equations and difference equations.</td>
</tr>
<tr>
<td>Lecture 16</td>
<td>Characterization of causality and stability of linear shift-invariant systems.</td>
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<tr>
<td>Lecture 17</td>
<td>System representation through differential equations and difference equations.</td>
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<tr>
<td>Lecture 18</td>
<td>Periodic and semi-periodic inputs to an LSI system</td>
</tr>
<tr>
<td>Lecture 19</td>
<td>The notion of a frequency response.</td>
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<td>Lecture 20</td>
<td>Its relation to the impulse response</td>
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<td>Lecture 21</td>
<td>Fourier series representation</td>
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<td>Lecture 22</td>
<td>Fourier Transform</td>
</tr>
<tr>
<td>Lecture 23</td>
<td>Convolution/multiplication and their effect in the frequency</td>
</tr>
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<td>Lecture</td>
<td>Topic</td>
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<td>24</td>
<td>Magnitude and phase response</td>
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<td>25</td>
<td>Fourier domain duality.</td>
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<td>26</td>
<td>The Discrete-Time Fourier Transform (DTFT) and Discrete Fourier Transform (DFT).</td>
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<tr>
<td>27</td>
<td>Parseval's Theorem. The idea of signal space and orthogonal bases</td>
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<td>28</td>
<td>The Laplace Transform</td>
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<tr>
<td>29</td>
<td>Notion of eigen functions of LSI systems</td>
</tr>
<tr>
<td>30</td>
<td>A basis of eigen functions, region of convergence</td>
</tr>
<tr>
<td>31</td>
<td>Poles and zeros of system, Laplace domain analysis,</td>
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<tr>
<td>32</td>
<td>Solution to differential equations and system behavior.</td>
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<tr>
<td>33</td>
<td>The z-Transform for discrete time signals and systems- eigen functions,</td>
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<tr>
<td>34</td>
<td>Region of convergence, z-domain analysis.</td>
</tr>
<tr>
<td>35</td>
<td>State-space analysis and multi-input, multi-output representation.</td>
</tr>
<tr>
<td>36</td>
<td>The state-transition matrix and its role.</td>
</tr>
<tr>
<td>37</td>
<td>The Sampling Theorem and its implications- Spectra of sampled signals.</td>
</tr>
<tr>
<td>38</td>
<td>Reconstruction: ideal interpolator, zero-order hold, first-order hold, and so on</td>
</tr>
<tr>
<td>39</td>
<td>Aliasing and its effects.</td>
</tr>
<tr>
<td>40</td>
<td>Relation between continuous and discrete time systems.</td>
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</tbody>
</table>

**Content delivery method:**

1. Chalk and Duster
2. PPT
3. Animation
4. Hand-outs
Assignment 3

For each of the following signals, determine whether it is even, odd, or neither.

(a) 

![Figure P2.4-1](image)

(b) 

![Figure P2.4-2](image)

(c) 

![Figure P2.4-3](image)

(d) 

![Figure P2.4-4](image)

Q1.
Evaluate the following sums:

(a) \[ \sum_{n=0}^{5} 2 \left( \frac{3}{a} \right)^n \]

(b) \[ \sum_{n=2}^{6} b^n \]

(c) \[ \sum_{n=0}^{\infty} \left( \frac{2}{3} \right)^n \]

*Hint: Convert each sum to the form* \[ C \sum_{n=0}^{N-1} \alpha^n = S_N \quad \text{or} \quad C \sum_{n=0}^{\infty} \alpha^n = S_\infty \]

and use the formulas \[ S_N = C \left( \frac{1 - \alpha^N}{1 - \alpha} \right), \quad S_\infty = \frac{C}{1 - \alpha} \quad \text{for } |\alpha| < 1 \]

Q2.

The first-order difference equation \( y[n] - ay[n - 1] = x[n], 0 < a < 1, \) describes a particular discrete-time system initially at rest.

(a) Verify that the impulse response \( h[n] \) for this system is \( h[n] = a^n u[n] \).

(b) Is the system

(i) memoryless?

(ii) causal?

(iii) stable?

Clearly state your reasoning.

(c) Is this system stable if \( |a| > 1 \)?

Q3.
Assignment 4

Consider a discrete-time system with impulse response

\[ h[n] = (\frac{1}{2})^n u[n] \]

Determine the response to each of the following inputs:

(a) \( x[n] = (-1)^n = e^{jn} \) for all \( n \)

(b) \( x[n] = e^{jn/4} \) for all \( n \)

(c) \( x[n] = \cos \left( \frac{\pi n}{4} + \frac{\pi}{8} \right) \) for all \( n \)

Q1.

Consider two specific periodic sequences \( \bar{x}[n] \) and \( \bar{y}[n] \). \( \bar{x}[n] \) has period \( N \) and \( \bar{y}[n] \) has period \( M \). The sequence \( \bar{v}[n] \) is defined as \( \bar{v}[n] = \bar{x}[n] + \bar{y}[n] \).

(a) Show that \( \bar{v}[n] \) is periodic with period \( MN \).

(b) Since \( \bar{x}[n] \) has period \( N \), its discrete Fourier series coefficients \( a_k \) also have period \( N \). Similarly, since \( \bar{y}[n] \) has period \( M \), its discrete Fourier series coefficients \( b_k \) also have period \( M \). The discrete Fourier series coefficients of \( \bar{v}[n] \), \( c_k \), have period \( MN \). Determine \( c_k \) in terms of \( a_k \) and \( b_k \).

Q2.

The sequence \( x[n] = (-1)^n \) is obtained by sampling the continuous-time sinusoidal signal \( x(t) = \cos \omega_0 t \) at 1-ms intervals, i.e.,

\[ \cos(\omega_0 nT) = (-1)^n, \quad T = 10^{-3} \text{ s} \]

Determine three distinct possible values of \( \omega_0 \).

Q3.
### 3EI4-06: Network Theory

**4 Credits**  
**3L:1T:0P**  
**Max. Marks: 100 (IA:30, ETE:70)**  
**End Term Exam: 3 Hours**

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<tr>
<th>SN</th>
<th>Contents</th>
<th>Hours</th>
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<tbody>
<tr>
<td>1</td>
<td>Node and Mesh Analysis, matrix approach of network containing voltage and current sources, and reactances, source transformation and duality.</td>
<td>7</td>
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<tr>
<td>2</td>
<td>Network theorems: Superposition, reciprocity, Thevenin’s, Norton’s, Maximum power Transfer, compensation and Tallegen's theorem as applied to AC. circuits.</td>
<td>7</td>
</tr>
<tr>
<td>3</td>
<td>Trigonometric and exponential Fourier series: Discrete spectra and symmetry of waveform, steady state response of a network to non-sinusoidal periodic inputs, power factor, effective values, Fourier transform and continuous spectra, three phase unbalanced circuit and power calculation.</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>Laplace transforms and properties: Partial fractions, singularity functions, waveform synthesis, analysis of RC, RL, and RLC networks with and without initial conditions with Laplace transforms evaluation of initial conditions.</td>
<td>8</td>
</tr>
<tr>
<td>5</td>
<td>Transient behavior, concept of complex frequency, Driving points and transfer functions poles and zeros of immittance function, their properties, sinusoidal response from pole-zero locations, convolution theorem and Two four port network and interconnections, Behaviors of series and parallel resonant circuits, Introduction to band pass, low pass, high pass and band reject filters.</td>
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**Total**  
40
### Course Outcome:

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<td>Network Theory</td>
<td>CO 1</td>
<td>Apply the basic circuital law and simplify the network using network theorems</td>
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<td>CO 2</td>
<td>Appreciate the frequency domain techniques in different applications.</td>
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<td>CO 3</td>
<td>Apply Laplace Transform for steady state and transient analysis</td>
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<td>CO 4</td>
<td>Evaluate transient response and two-port network parameters</td>
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<td>CO 5</td>
<td>Analyze the series resonant and parallel resonant circuit and design filters</td>
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### CO-PO Mapping:

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3: Strongly  2: Moderate  1: Weak
## Lecture Plan:

<table>
<thead>
<tr>
<th>Lecture No.</th>
<th>Content to be taught</th>
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<tbody>
<tr>
<td>Lecture 1</td>
<td>Overview of Network Theory and its significance</td>
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<td>Lecture 2</td>
<td>Node and Mesh Analysis</td>
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<tr>
<td>Lecture 3</td>
<td>matrix approach of network containing voltage and current sources and reactances</td>
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<td>Lecture 4</td>
<td>source transformation and duality</td>
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<tr>
<td>Lecture 5</td>
<td>Network theorems: Superposition and reciprocity</td>
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<td>Lecture 6</td>
<td>Thevenin’s and Norton’s theorem</td>
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<td>Lecture 7</td>
<td>Maximum power Transfer theorem</td>
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<td>Lecture 8</td>
<td>compensation and Tallegen’s theorem as applied to AC. Circuits</td>
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<tr>
<td>Lecture 9</td>
<td>Trigonometric and exponential Fourier series</td>
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<td>Fourier series: Discrete spectra and symmetry of waveform</td>
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<td>Lecture 11</td>
<td>Steady state response of a network to non-sinusoidal periodic inputs</td>
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<td>Lecture 12</td>
<td>power factor and effective values</td>
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<td>Lecture 13</td>
<td>Fourier transform and continuous spectra</td>
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<td>Lecture 14</td>
<td>three phase unbalanced circuit and power calculation</td>
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<td>Lecture 15</td>
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<td>Lecture 17</td>
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<td>analysis of RC networks</td>
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<td>Lecture 21</td>
<td>analysis of RL networks</td>
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<td>analysis of RLC networks</td>
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<td>Lecture 23</td>
<td>Analysis of networks with and without initial conditions</td>
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<td>Lecture 24</td>
<td>Analysis of networks with and without initial conditions</td>
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<td>Lecture 25</td>
<td>Analysis of networks with and without initial conditions with laplace transforms evaluation</td>
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<td>Lecture 26</td>
<td>Analysis of networks with and without initial conditions with laplace transforms evaluation of initial condition</td>
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<td>Lecture 27</td>
<td>Transient behavior</td>
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<td>Lecture 29</td>
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<tr>
<td>Lecture 30</td>
<td>Driving points and transfer functions poles and zeros of immittance function: their properties</td>
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<td>Lecture 31</td>
<td>sinusoidal response from pole-zero locations</td>
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<tr>
<td>32</td>
<td>sinusoidal response from pole-zero locations</td>
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<td>33</td>
<td>convolution theorem</td>
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<td>sinusoidal response from pole-zero locations</td>
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<td>35</td>
<td>Two four port network and interconnections</td>
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<td>36</td>
<td>Two four port network and interconnections</td>
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<tr>
<td>37</td>
<td>Behaviors of series and parallel resonant circuits</td>
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<tr>
<td>38</td>
<td>Introduction to band pass and low pass</td>
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<td>39</td>
<td>Introduction to high pass and reject filters</td>
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<td>40</td>
<td>Spill over class</td>
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**Content delivery method:**
1. Chalk and Duster
2. PPT
3. Hand-outs
### Sample assignments:

<table>
<thead>
<tr>
<th>Assignment 1</th>
<th>Q1. Elaborate the significance of source transformation with relevant example</th>
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<tbody>
<tr>
<td></td>
<td>Q2. State and prove time differentiation theorem in Laplace Transform</td>
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<tr>
<td></td>
<td>Q3. Find the Thevenin equivalent of the network shown in figure. What power would be delivered to a load of 100 ohms at a and b?</td>
</tr>
<tr>
<td>Assignment 2</td>
<td>Q4. Calculate Thevenin equivalent circuit with respect to terminals a and b</td>
</tr>
<tr>
<td></td>
<td>Q5. Derive transient current and voltage responses of sinusoidal driven RL and RC circuits.</td>
</tr>
<tr>
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<td>Q6. Specify the restrictions on pole and zero locations for transfer functions and driving-point functions.</td>
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</table>
## 3EI4-07: Electronic Devices

**4 Credits**  
**Max. Marks:** 100 (IA:30, ETE:70)  
**End Term Exam:** 3 Hours

<table>
<thead>
<tr>
<th>SN</th>
<th>Contents</th>
<th>Hours</th>
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<tbody>
<tr>
<td>1</td>
<td>Introduction to Semiconductor Physics: Introduction, Energy band gap structures of semiconductors, Classifications of semiconductors, Degenerate and non-degenerate semiconductors, Direct and indirect band gap semiconductors, Electronic properties of Silicon, Germanium, Compound Semiconductor, Gallium Arsenide, Gallium phosphide &amp; Silicon carbide, Variation of semiconductor conductivity, resistance and bandgap with temperature and doping. Thermistors, Sensitors.</td>
<td>6</td>
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<tr>
<td>2</td>
<td>Review of Quantum Mechanics, Electrons in periodic Lattices, E-k diagrams. Energy bands in intrinsic and extrinsic silicon; Carrier transport: diffusion current, drift current, mobility and resistivity; sheet resistance, design of resistors.</td>
<td>6</td>
</tr>
<tr>
<td>3</td>
<td>Generation and recombination of carriers; Poisson and continuity equation P-N junction characteristics, I-V characteristics, and small signal switching models; Avalanche breakdown, Zener diode, Schottky diode.</td>
<td>8</td>
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<tr>
<td>4</td>
<td>Bipolar Junction Transistor, I-V characteristics, Ebers-Moll Model, MOS capacitor, C-V characteristics, MOSFET, I-V characteristics, and small signal models of MOS transistor, LED, photodiode and solar cell.</td>
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<tr>
<td>5</td>
<td>Integrated circuit fabrication process: oxidation, diffusion, ion implantation, Photolithography, etching, chemical vapor deposition, sputtering, twin-tub CMOS process.</td>
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**Course Outcome:**

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<tr>
<td>3EI4-07</td>
<td>Electronic Devices</td>
<td>CO 1</td>
<td>Understanding the semiconductor physics of the intrinsic, P and N materials.</td>
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<td>CO 2</td>
<td>Understanding the characteristics of current flow in a bipolar junction transistor and MOSFET.</td>
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<td>CO 3</td>
<td>Understand and utilize the mathematical models of semiconductor junctions and MOS transistors for circuits and systems.</td>
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<td>CO 4</td>
<td>Analyze the characteristics of different electronic devices such as Amplifiers, LEDs, Solar cells, etc.</td>
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<td>CO 5</td>
<td>Theoretical as well as experimental understanding of Integrated circuit fabrication.</td>
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**CO-PO Mapping:**

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3: Strongly  2: Moderate  1: Weak
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<td>E-k diagrams</td>
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<td>Energy bands in intrinsic and extrinsic silicon</td>
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<td>Lecture 9</td>
<td>Carrier transport: diffusion current, drift current, mobility and resistivity</td>
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<td>Sheet resistance and design of resistors</td>
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<td>Generation and recombination of carriers</td>
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<td>Poisson and continuity equation</td>
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<td>P-N junction characteristics and their I-V characteristics</td>
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<td>P-N junction small signal switching models</td>
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<tr>
<td>Lecture 17</td>
<td>Avalanche breakdown</td>
</tr>
<tr>
<td>Lecture 18</td>
<td>Zener diode and Schottky diode</td>
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<tr>
<td>Lecture 19</td>
<td>Basics of Bipolar Junction Transistor</td>
</tr>
<tr>
<td>Lecture 20</td>
<td>I-V characteristics of BJT</td>
</tr>
<tr>
<td>Lecture 21</td>
<td>Ebers-Moll Model</td>
</tr>
<tr>
<td>Lecture 22</td>
<td>MOS capacitor</td>
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<tr>
<td>Lecture 23</td>
<td>MOS capacitor</td>
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<tr>
<td>Lecture 24</td>
<td>C-V characteristics</td>
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<td>Lecture 25</td>
<td>Basics of MOSFET</td>
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<td>Lecture 26</td>
<td>Basics of MOSFET</td>
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<tr>
<td>Lecture 27</td>
<td>I-V characteristics of MOSFET</td>
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<tr>
<td>Lecture 28</td>
<td>Small signal models of MOS transistor</td>
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<tr>
<td>Lecture 29</td>
<td>Small signal models of MOS transistor</td>
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<tr>
<td>Lecture 30</td>
<td>Light Emitting Diode</td>
</tr>
<tr>
<td>Lecture 31</td>
<td>Photodiode and solar cell</td>
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<tr>
<td>Lecture 32</td>
<td>Basics of Integrated Circuits</td>
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<tr>
<td>Lecture 33</td>
<td>Advancement in Integrated Circuits</td>
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<tr>
<td>Lecture 34</td>
<td>Oxidation, diffusion and ion implantation</td>
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<tr>
<td>Lecture 35</td>
<td>Photolithography and etching</td>
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<tr>
<td>Lecture 36</td>
<td>Chemical vapor deposition</td>
</tr>
<tr>
<td>Lecture 37</td>
<td>Sputtering</td>
</tr>
<tr>
<td>Lecture 38</td>
<td>Twin-tub CMOS process</td>
</tr>
<tr>
<td>Lecture 39</td>
<td>Spill over class</td>
</tr>
<tr>
<td>Lecture 40</td>
<td>Spill over class</td>
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</table>

**Content delivery method:**

1. Chalk and Duster
2. PPT
3. Hand-outs
Sample assignments:

<table>
<thead>
<tr>
<th>Assignment 1</th>
<th>Q1. Investigates the input/output characteristics of various diodes?</th>
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<tbody>
<tr>
<td></td>
<td>Q2. Investigate the applications of various diodes?</td>
</tr>
<tr>
<td></td>
<td>Q3. A p-type sample of silicon has a resistivity of 5 Ω-cm. In this sample, the hole mobility, ( \mu_h ), is 600 cm(^2)/V-s and the electron mobility, ( \mu_e ), is 1600 cm(^2)/V-s. Ohmic contacts are formed on the ends of the sample and a uniform electric field is imposed which results in a drift current density in the sample is ( 2 \times 10^3 ) A/cm(^2).</td>
</tr>
<tr>
<td></td>
<td>[1]. What are the hole and electron concentrations in this sample?</td>
</tr>
<tr>
<td></td>
<td>[2]. What are the hole and electron drift velocities under these conditions?</td>
</tr>
<tr>
<td></td>
<td>[3]. What is the magnitude of the electric field?</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Assignment 2</th>
<th>Q1. Discuss the applications of Ebers-Moll Model.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Q2. Discuss different types of fabrication techniques.</td>
</tr>
<tr>
<td></td>
<td>Q3. Discuss various characteristics of CMOS transistor.</td>
</tr>
</tbody>
</table>
### 3EI4-21: Electronics Devices Lab

**1 Credit**  
**Max. Marks:** 100 (IA:60, ETE:40)  
**OL:0T:2P**

#### List of Experiments

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Name of Experiment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Study the following devices: (a) Analog &amp; digital multimeters (b) Function/Signal generators (c) Regulated d. c. power supplies (constant voltage and constant current operations) (d) Study of analog and digital CRO, measurement of time period, amplitude, frequency &amp; phase angle using Lissajous figures.</td>
</tr>
<tr>
<td>2.</td>
<td>Plot V-I characteristic of P-N junction diode &amp; calculate cut-in voltage, reverse Saturation current and static &amp; dynamic resistances.</td>
</tr>
<tr>
<td>3.</td>
<td>Plot the output waveform of half wave rectifier and effect of filters on waveform. Also calculate its ripple factor.</td>
</tr>
<tr>
<td>4.</td>
<td>Study bridge rectifier and measure the effect of filter network on D.C. voltage output &amp; ripple factor.</td>
</tr>
<tr>
<td>5.</td>
<td>Plot and verify output waveforms of different clipper and clamper.</td>
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<tr>
<td>6.</td>
<td>Plot V-I characteristic of Zener diode</td>
</tr>
<tr>
<td>7.</td>
<td>Study of Zener diode as voltage regulator. Observe the effect of load changes and determine load limits of the voltage regulator</td>
</tr>
<tr>
<td>8.</td>
<td>Plot input-output characteristics of BJT in CB, CC and CE configurations. Find their h-parameters.</td>
</tr>
<tr>
<td>9.</td>
<td>Study of different biasing circuits of BJT amplifier and calculate its Q-point.</td>
</tr>
<tr>
<td>11.</td>
<td>Plot input-output characteristics of field effect transistor and measure $I_{\text{dss}}$ and $V_p$.</td>
</tr>
<tr>
<td>12.</td>
<td>Plot frequency response curve for FET amplifier and calculate its gain bandwidth product.</td>
</tr>
</tbody>
</table>
### Course Outcome:

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Name</th>
<th>Course Outcome</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>3EI4-21</td>
<td>Electronic Devices Lab</td>
<td>CO 1</td>
<td>Understand the characteristics of different Electronic Devices.</td>
</tr>
<tr>
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<td></td>
<td>CO 2</td>
<td>Verify the rectifier circuits using diodes and implement them using hardware.</td>
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<tr>
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<td>CO 3</td>
<td>Design various amplifiers like CE, CC, common source amplifiers and implement them using hardware and also observe their frequency responses</td>
</tr>
<tr>
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<td>CO 4</td>
<td>Understand the construction, operation and characteristics of JFET and MOSFET, which can be used in the design of amplifiers.</td>
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<tr>
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<td>CO 5</td>
<td>Understand the need and requirements to obtain frequency response from a transistor so that Design of RF amplifiers and other high frequency amplifiers is feasible</td>
</tr>
</tbody>
</table>

**CO-PO Mapping:**

<table>
<thead>
<tr>
<th>Subject</th>
<th>Course Outcomes</th>
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</tbody>
</table>

3: Strongly 2: Moderate 1: Weak
### 3EI4-22: Digital System Design Lab

**1 Credit**  
**OL:0T:2P**  
**Max. Marks: 100 (IA:60, ETE:40)**

#### List of Experiments

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Name of Experiment</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Part A: Combinational Circuits</strong></td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td>To verify the truth tables of logic gates: AND, OR, NOR, NAND, NOR, Ex-OR and Ex-NOR</td>
</tr>
<tr>
<td>2.</td>
<td>To verify the truth table of OR, AND, NOR, Ex-OR, Ex-NOR logic gates realized using NAND &amp; NOR gates.</td>
</tr>
<tr>
<td>3.</td>
<td>To realize an SOP and POS expression.</td>
</tr>
<tr>
<td>4.</td>
<td>To realize Half adder/ Subtractor&amp; Full Adder/ Subtractor using NAND &amp; NOR gates and to verify their truth tables</td>
</tr>
<tr>
<td>5.</td>
<td>To realize a 4-bit ripple adder/ Subtractor using basic Half adder/ Subtractor &amp; basic Full Adder/ Subtractor.</td>
</tr>
<tr>
<td>6.</td>
<td>To design 4-to-1 multiplexer using basic gates and verify the truth table. Also verify the truth table of 8-to-1 multiplexer using IC</td>
</tr>
<tr>
<td>7.</td>
<td>To design 1-to-4 demultiplexer using basic gates and verify the truth table. Also to construct 1-to-8 demultiplexer using blocks of 1-to-4 demultiplexer</td>
</tr>
<tr>
<td>8.</td>
<td>To design 2x4 decoder using basic gates and verify the truth table. Also verify the truth table of 3x8 decoder using IC</td>
</tr>
<tr>
<td>9.</td>
<td>Design &amp; Realize a combinational circuit that will accept a 2421 BCD code and drive a TIL -312 seven-segment display</td>
</tr>
<tr>
<td><strong>Part B: Sequential Circuits</strong></td>
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<tr>
<td>10.</td>
<td>Using basic logic gates, realize the R-S, J-K and D-flip flops with and without clock signal and verify their truth table.</td>
</tr>
<tr>
<td>11.</td>
<td>Construct a divide by 2, 4 &amp; 8 asynchronous counter. Construct a 4-bit binary counter and ring counter for a particular output pattern using D flip flop.</td>
</tr>
<tr>
<td>12.</td>
<td>Design and construct unidirectional shift register and verify the</td>
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<tr>
<td>13.</td>
<td>Design and construct BCD ripple counter and verify the function.</td>
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<tr>
<td>14.</td>
<td>Design and construct a 4 Bit Ring counter and verify the function</td>
</tr>
<tr>
<td>15.</td>
<td>Perform input/output operations on parallel in/Parallel out and Serial in/Serial out registers using clock. Also exercise loading only one of multiple values into the register using multiplexer.</td>
</tr>
</tbody>
</table>

**Note:** Minimum 6 experiments to be conducted from **Part-A** & 4 experiments to be conducted from **Part-B**.
Course Outcome:

<table>
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<tr>
<th>Course Code</th>
<th>Course Name</th>
<th>Course Outcome</th>
<th>Details</th>
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<tbody>
<tr>
<td>3EI4-22</td>
<td>Digital System Design Lab</td>
<td>CO 1</td>
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<tr>
<td></td>
<td></td>
<td>CO 2</td>
<td>To minimize the complexity of digital logic circuits.</td>
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<tr>
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<td>CO 3</td>
<td>To design and analyse combinational logic circuits.</td>
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<tr>
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<td>CO 4</td>
<td>To design and analyse sequential logic circuits.</td>
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<td>CO 5</td>
<td>Able to implement applications of combinational &amp; sequential logic circuits.</td>
</tr>
</tbody>
</table>

CO-PO Mapping:

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<tr>
<th>Subject</th>
<th>Course Outcomes</th>
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</tbody>
</table>

3: Strongly  2: Moderate  1: Weak
### 3EI4-23: Signal Processing Lab

**1 Credit**

**Max. Marks: 100 (IA:60, ETE:40)**

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Name of Experiment (Simulate using MATLAB environment)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Generation of continuous and discrete elementary signals (periodic and non periodic) using mathematical expression.</td>
</tr>
<tr>
<td>2.</td>
<td>Generation of Continuous and Discrete Unit Step Signal.</td>
</tr>
<tr>
<td>3.</td>
<td>Generation of Exponential and Ramp signals in Continuous &amp; Discrete domain.</td>
</tr>
<tr>
<td>4.</td>
<td>Continuous and discrete time Convolution (using basic definition).</td>
</tr>
<tr>
<td>5.</td>
<td>Adding and subtracting two given signals. (Continuous as well as Discrete signals)</td>
</tr>
<tr>
<td>6.</td>
<td>To generate uniform random numbers between (0, 1).</td>
</tr>
<tr>
<td>7.</td>
<td>To generate a random binary wave.</td>
</tr>
</tbody>
</table>
| 8.      | To generate and verify random sequences with arbitrary distributions, means and variances for following:  
(a) Rayleigh distribution  
(b) Normal distributions: N(0,1).  
(c) Gaussian distributions: N (m, x) |
| 9.      | To plot the probability density functions. Find mean and variance for the above distributions |
Course Outcome:

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Name</th>
<th>Course Outcome</th>
<th>Details</th>
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<tbody>
<tr>
<td>3E14-23</td>
<td>Signal Processing Lab</td>
<td>CO 1</td>
<td>Able to generate different Continuous and Discrete time signals.</td>
</tr>
<tr>
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<td>CO 2</td>
<td>Understand the basics of signals and different operations on signals.</td>
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<td>CO 3</td>
<td>Develop simple algorithms for signal processing and test them using MATLAB</td>
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<tr>
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<td>CO 4</td>
<td>Able to generate the random signals having different distributions, mean and variance.</td>
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<tr>
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<td>CO 5</td>
<td>Design and conduct experiments, interpret and analyse data and report results.</td>
</tr>
</tbody>
</table>

CO-PO Mapping:

<table>
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<tr>
<th>Subject</th>
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<th>PO 1</th>
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3: Strongly  2: Moderate  1: Weak
### 3EI3-24: Computer Programming Lab-I

**1 Credit**

<table>
<thead>
<tr>
<th>Activities</th>
<th>Description</th>
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<tbody>
<tr>
<td>1.</td>
<td>Write a simple C program on a 32 bit compiler to understand the concept of array storage, size of a word. The program shall be written illustrating the concept of row major and column major storage. Find the address of element and verify it with the theoretical value. Program may be written for arrays upto 4-dimensions.</td>
</tr>
<tr>
<td>2.</td>
<td>Simulate a stack, queue, circular queue and dequeue using a one dimensional array as storage element. The program should implement the basic addition, deletion and traversal operations.</td>
</tr>
<tr>
<td>3.</td>
<td>Represent a 2-variable polynomial using array. Use this representation to implement addition of polynomials.</td>
</tr>
<tr>
<td>4.</td>
<td>Represent a sparse matrix using array. Implement addition and transposition operations using the representation.</td>
</tr>
<tr>
<td>5.</td>
<td>Implement singly, doubly and circularly connected linked lists illustrating operations like addition at different locations, deletion from specified locations and traversal.</td>
</tr>
<tr>
<td>6.</td>
<td>Repeat exercises 2, 3 &amp; 4 with linked structures.</td>
</tr>
<tr>
<td>7.</td>
<td>Implementation of binary tree with operations like addition, deletion, traversal.</td>
</tr>
<tr>
<td>8.</td>
<td>Depth first and breadth first traversal of graphs represented using adjacency matrix and list.</td>
</tr>
<tr>
<td>9.</td>
<td>Implementation of binary search in arrays and on linked Binary Search Tree.</td>
</tr>
<tr>
<td>10.</td>
<td>Implementation of insertion, quick, heap, topological and bubble sorting algorithms.</td>
</tr>
</tbody>
</table>

Max. Marks: 100 (IA:60, ETE:40)

OL:0T:2P